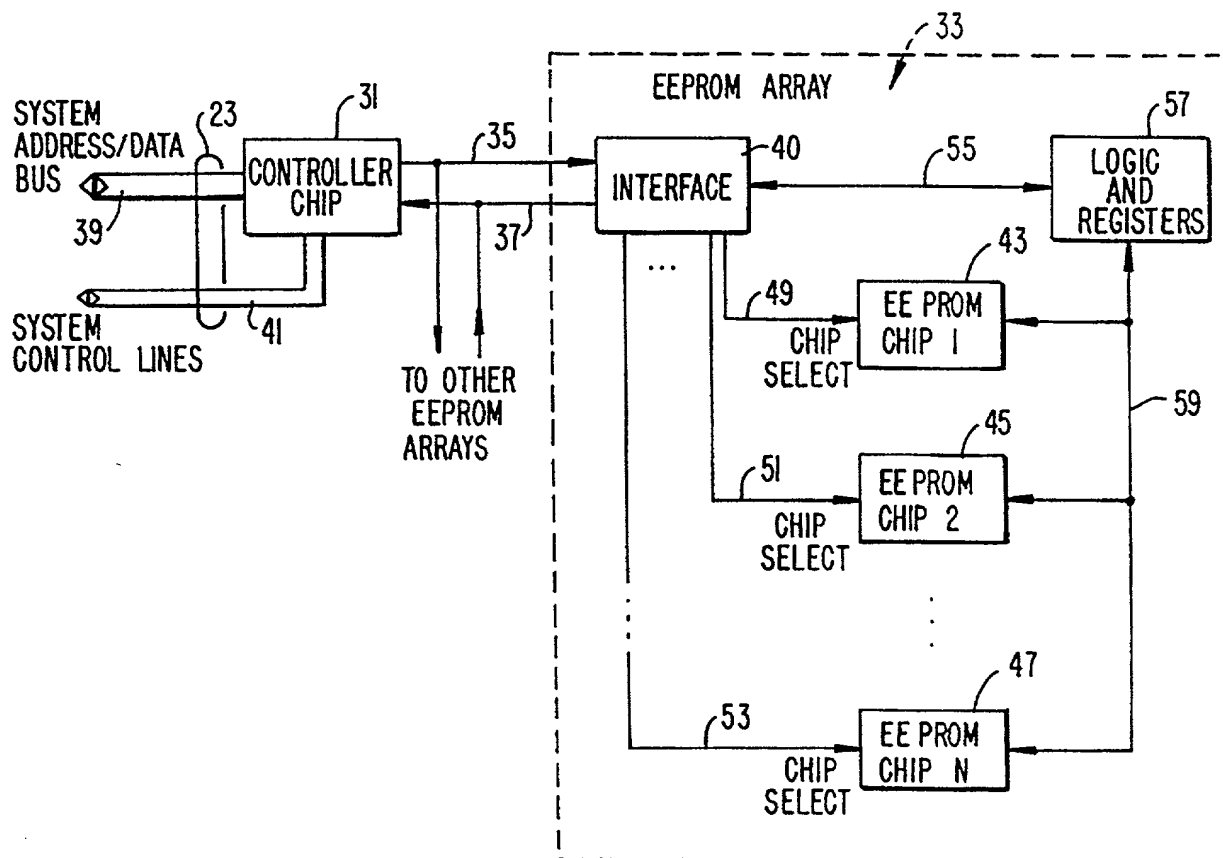
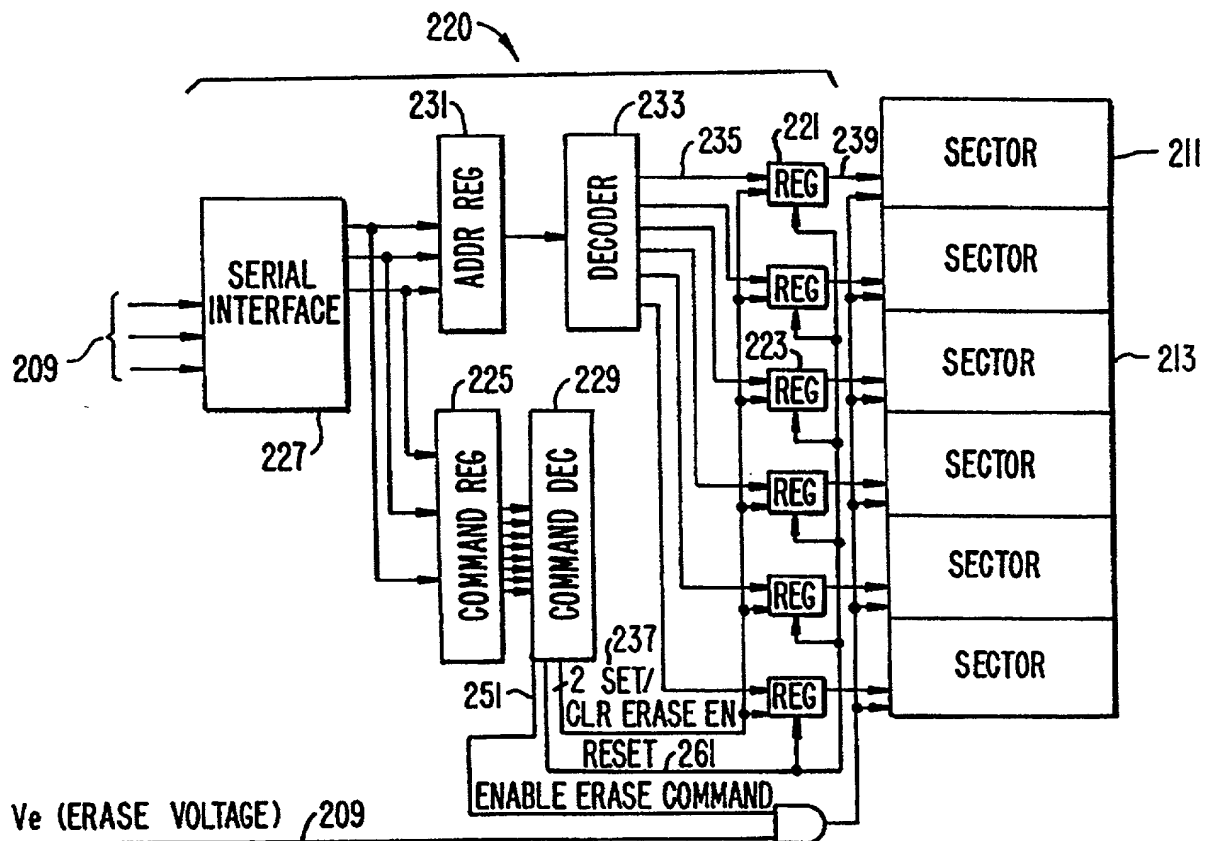
**FIG. 1A****FIG. 1B**



**FIG. 3B**



**FIG.\_3A**

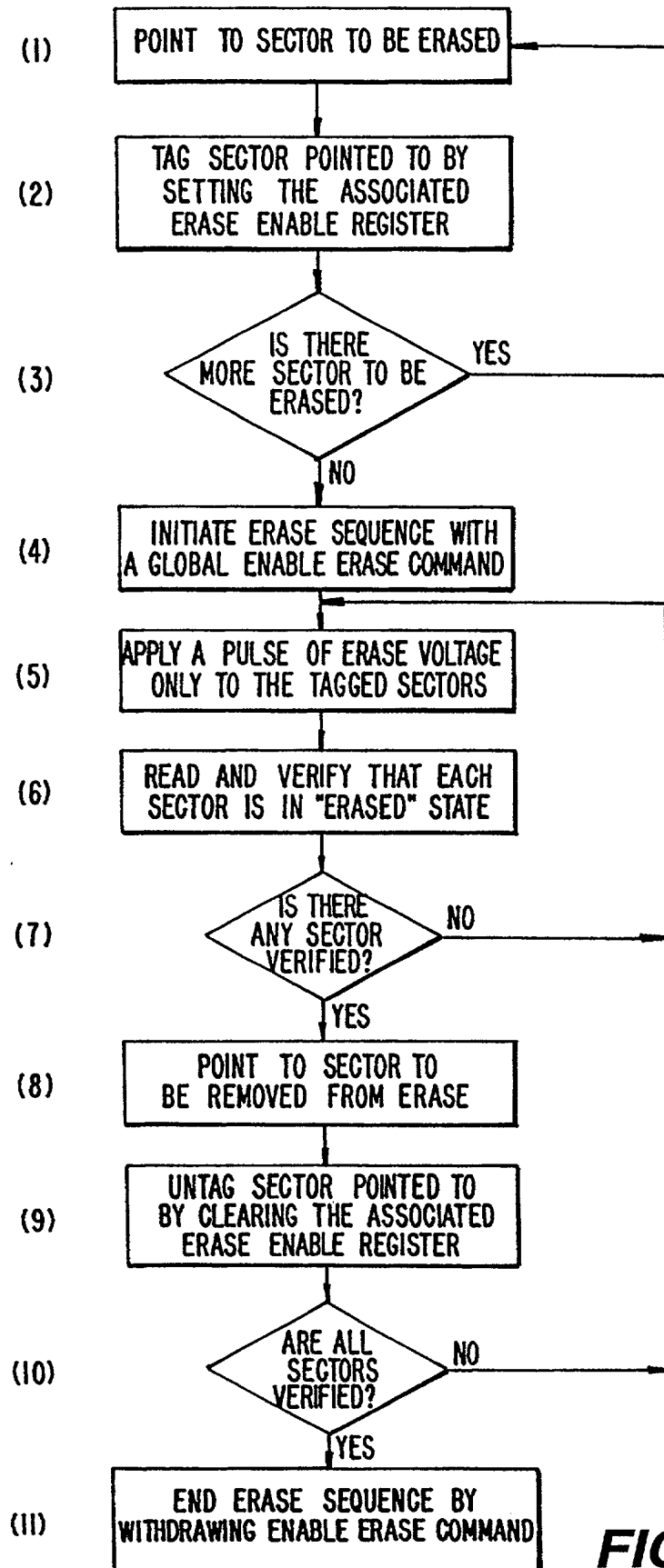
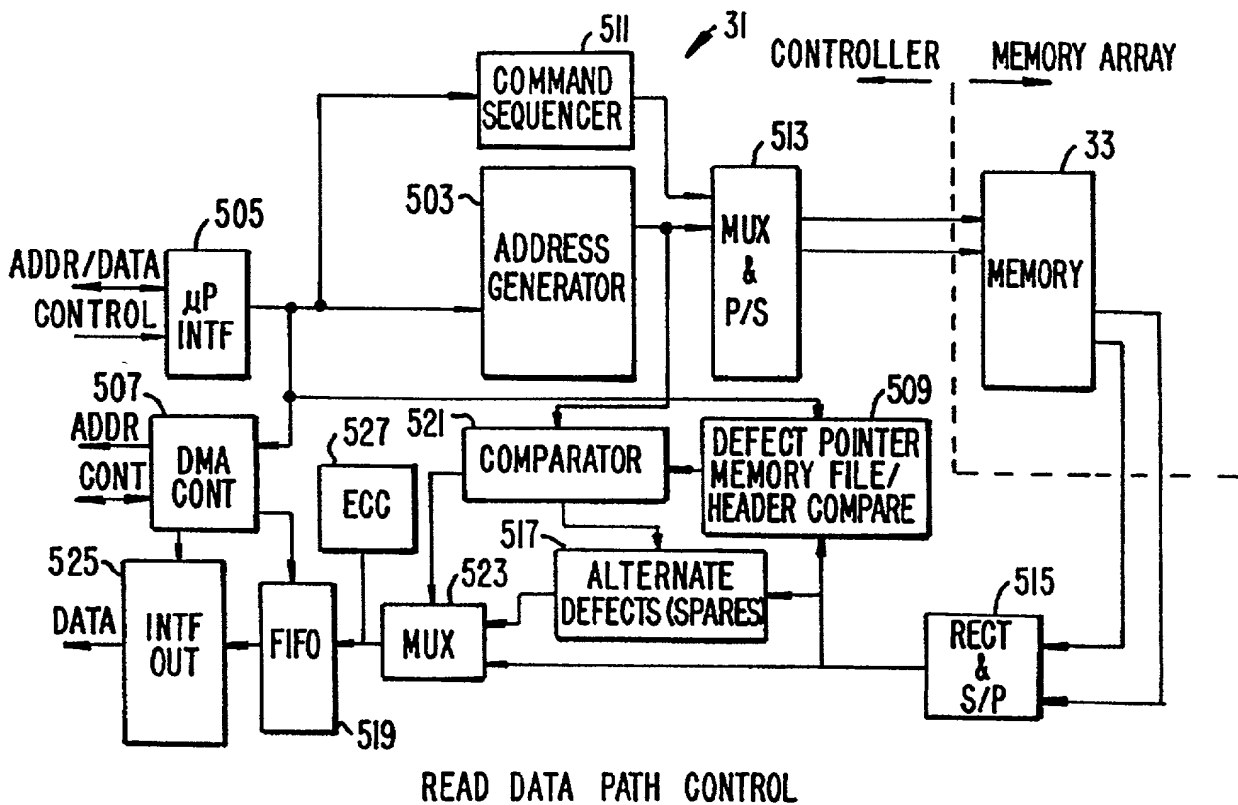
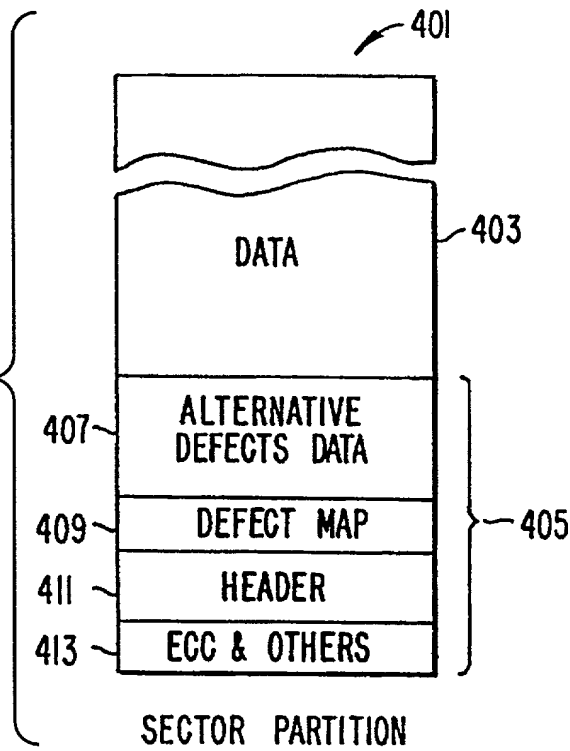
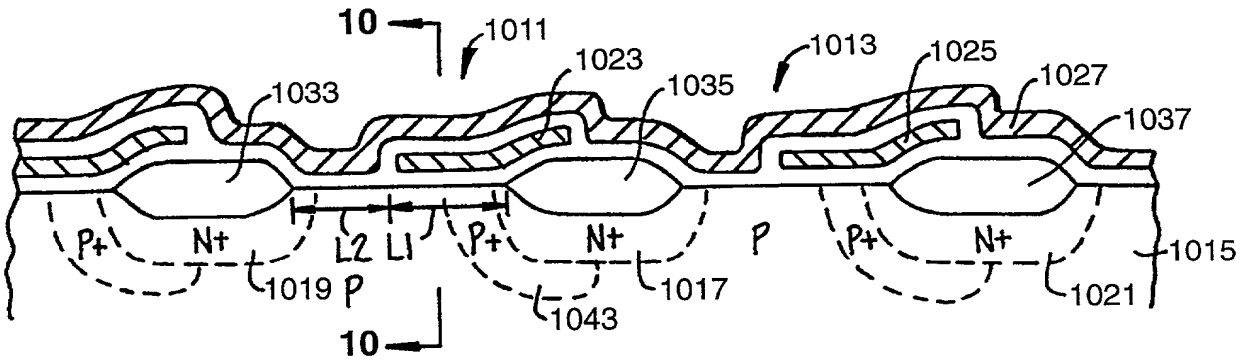


FIG. 4

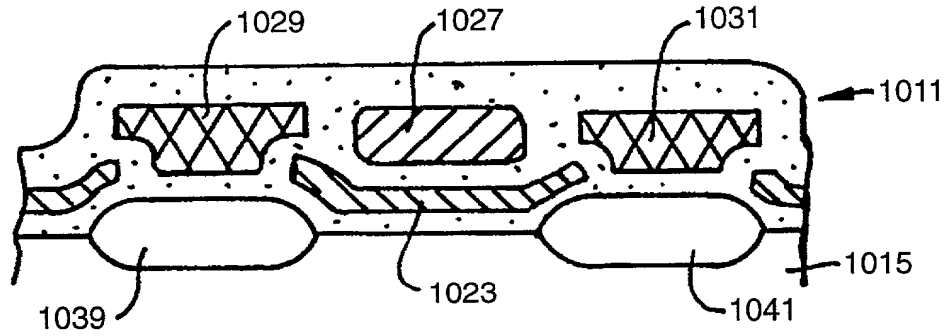
**FIG. 5****FIG. 6**



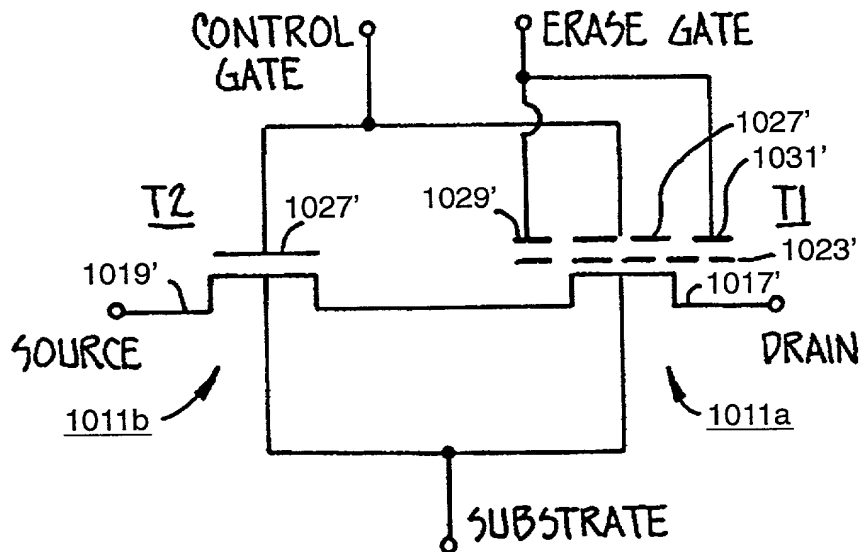
**FIG. 8**



**FIG. 9**



**FIG. 10**



**FIG. 11**

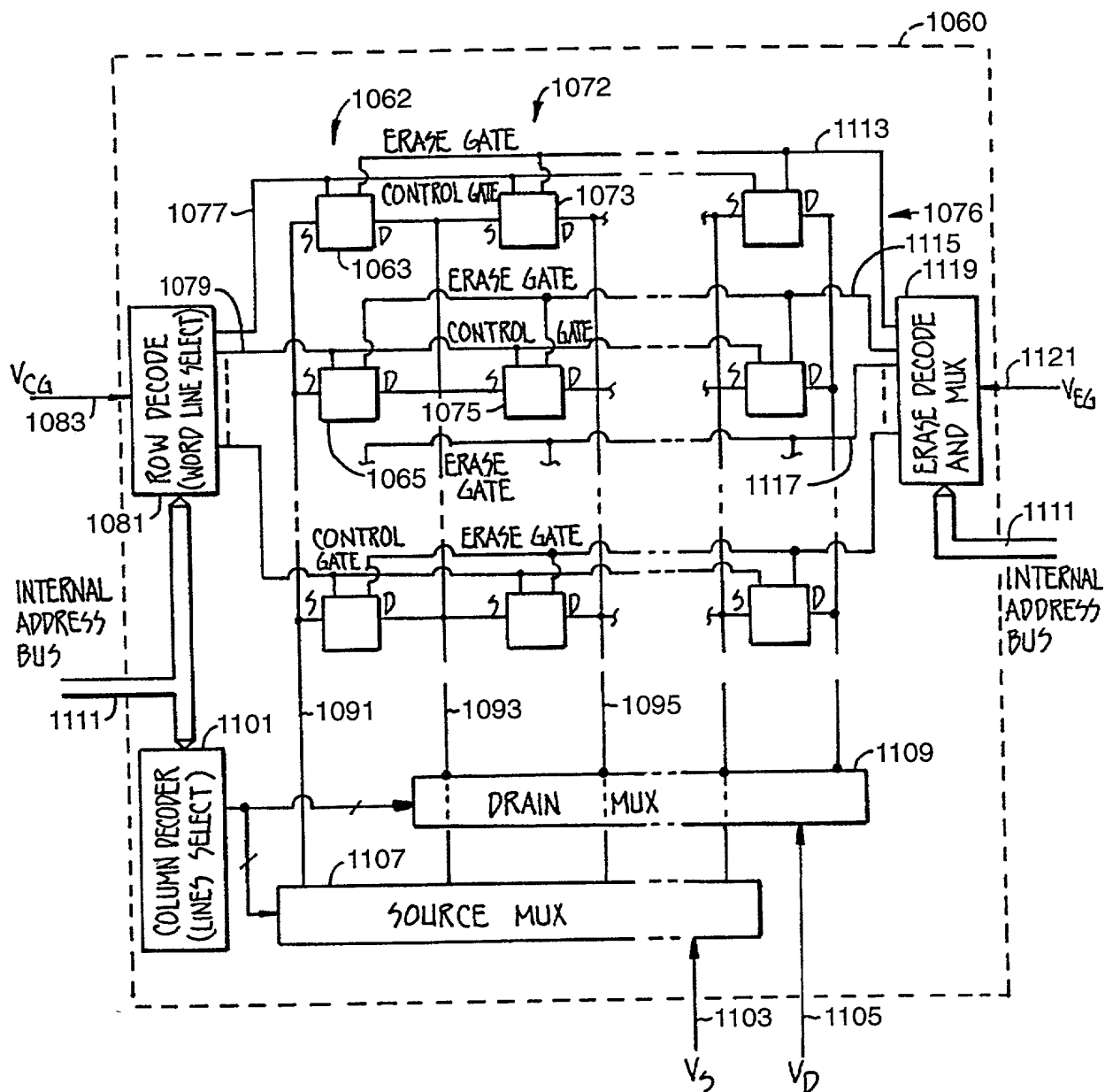


FIG. 12

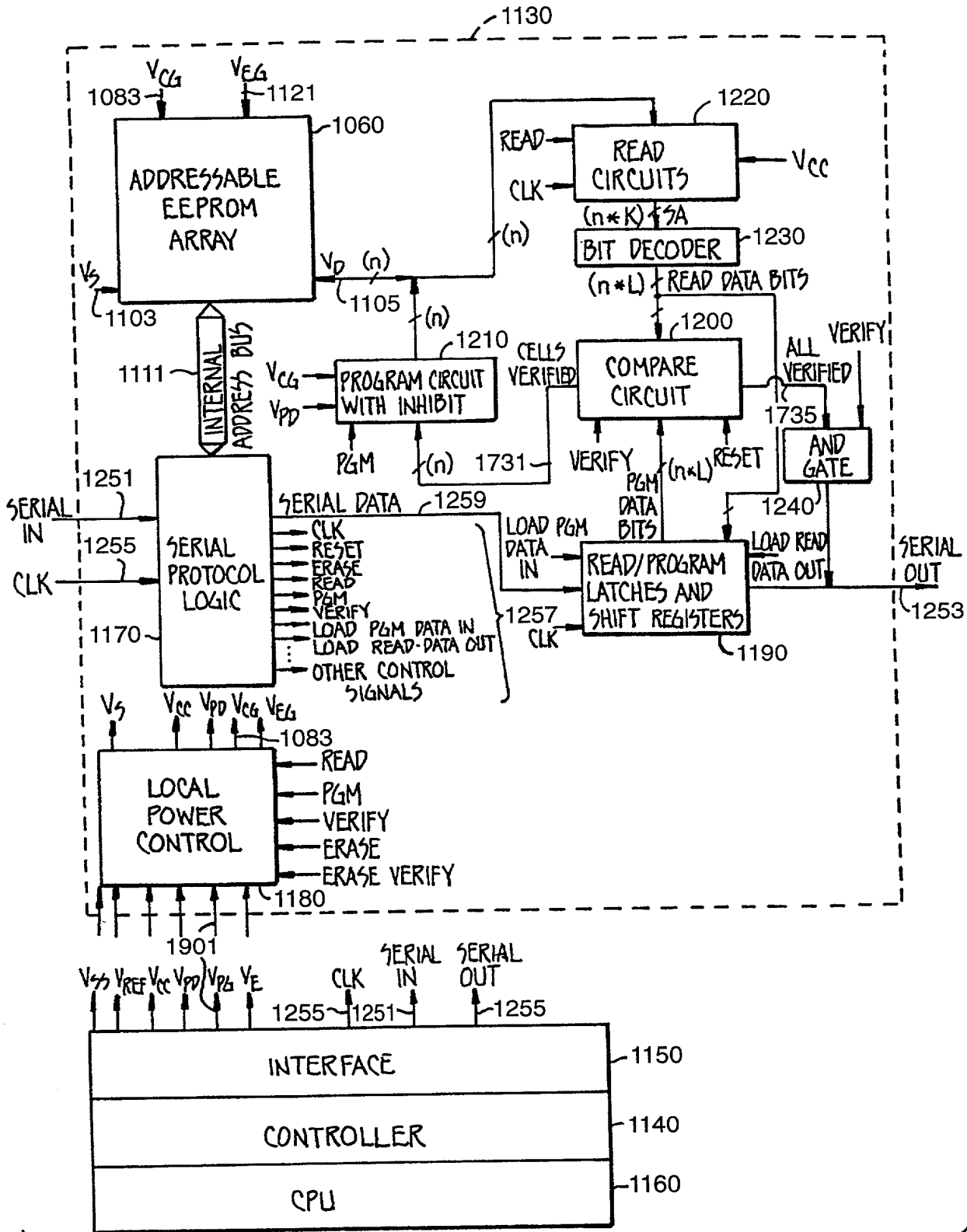


FIG. 13



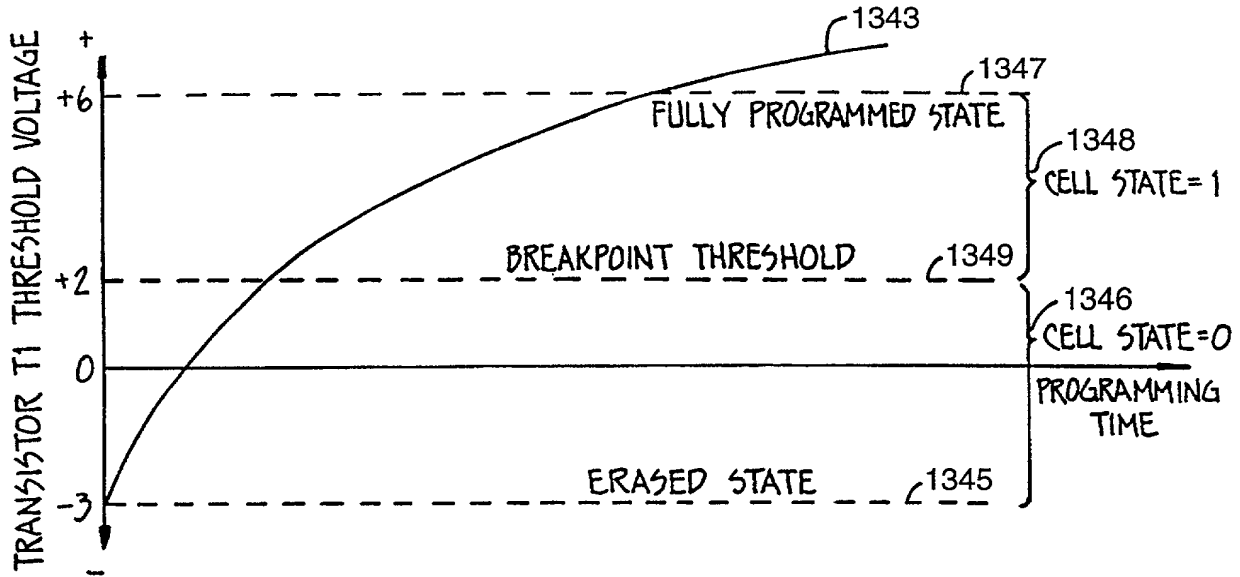


FIG. 14

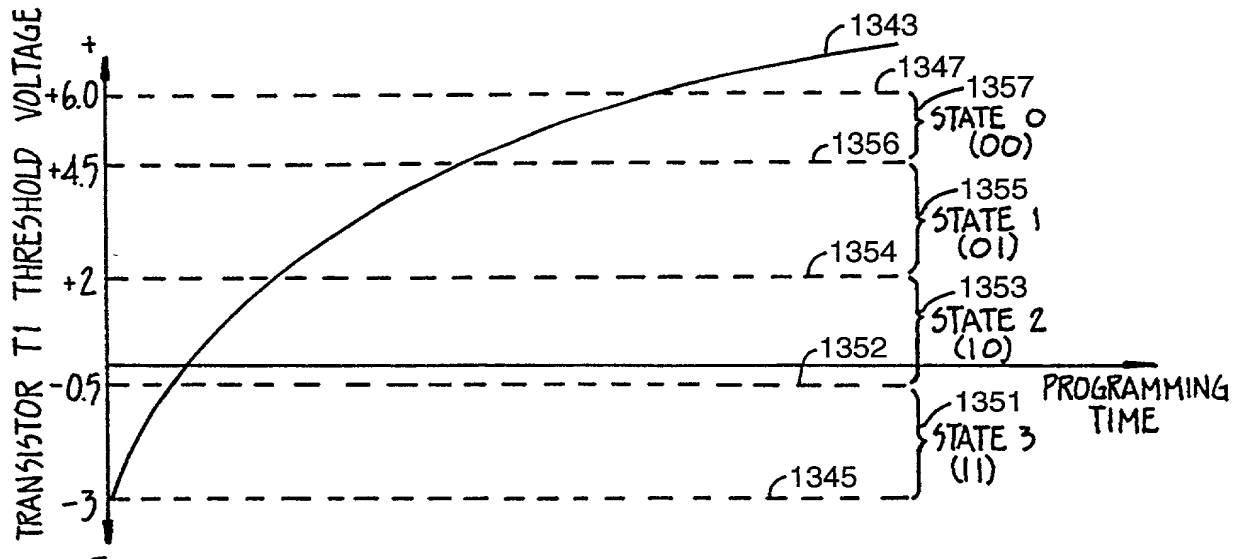


FIG. 15A

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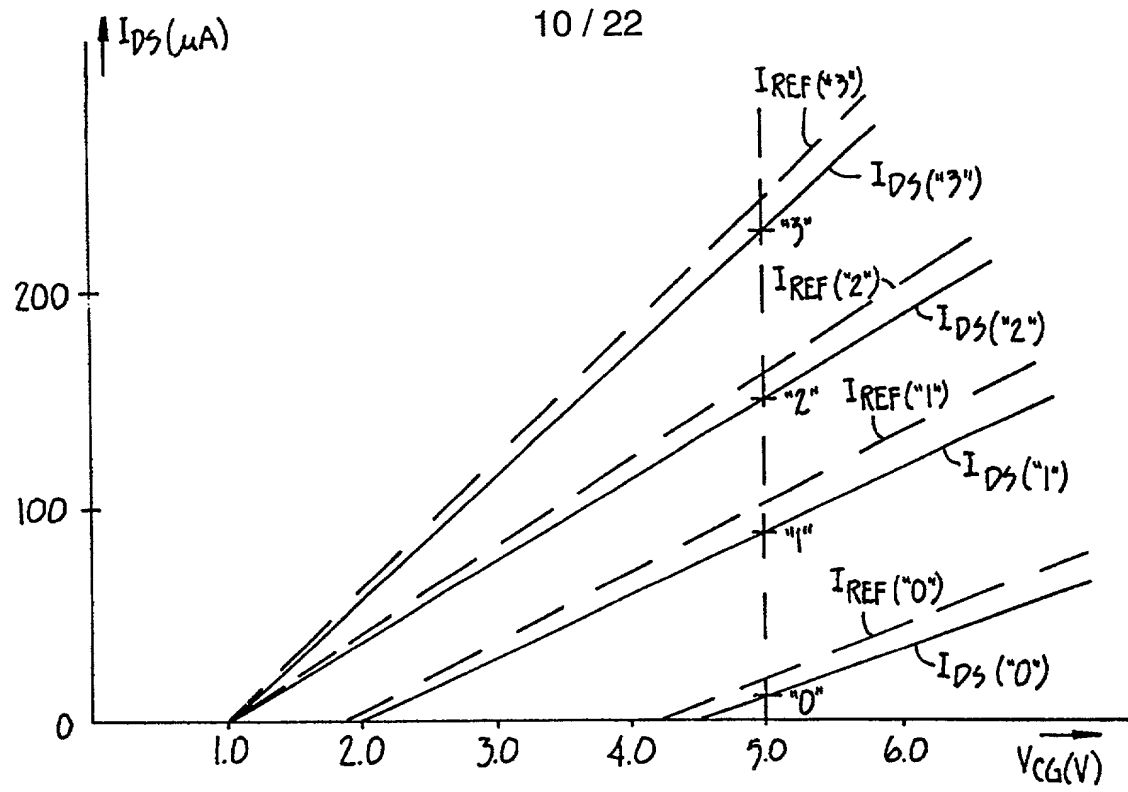


FIG. 15B

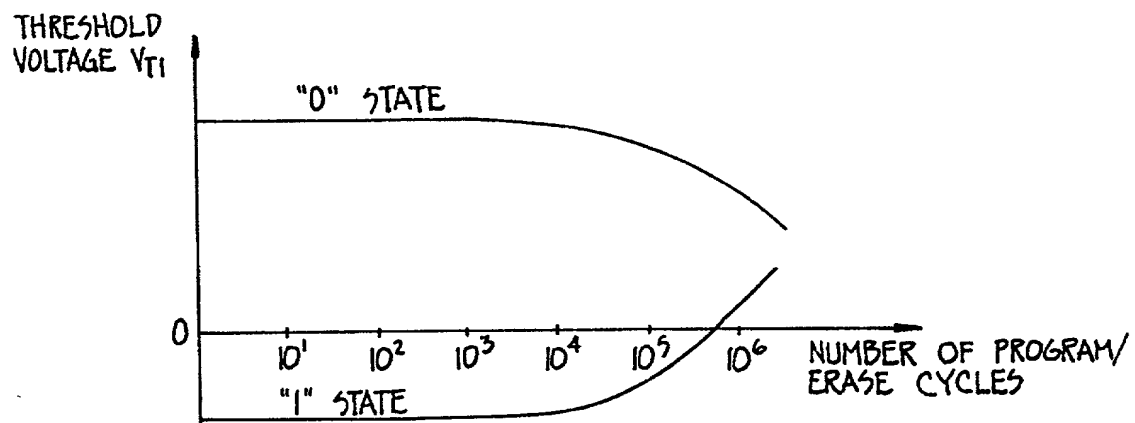


FIG. 16A

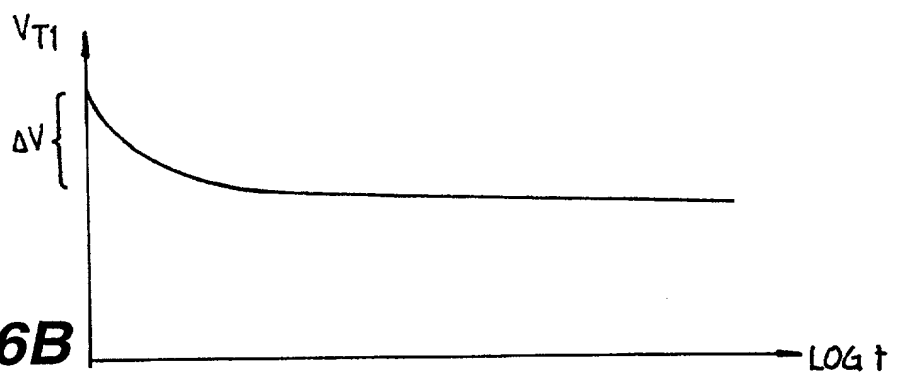


FIG. 16B

10050" 9879860

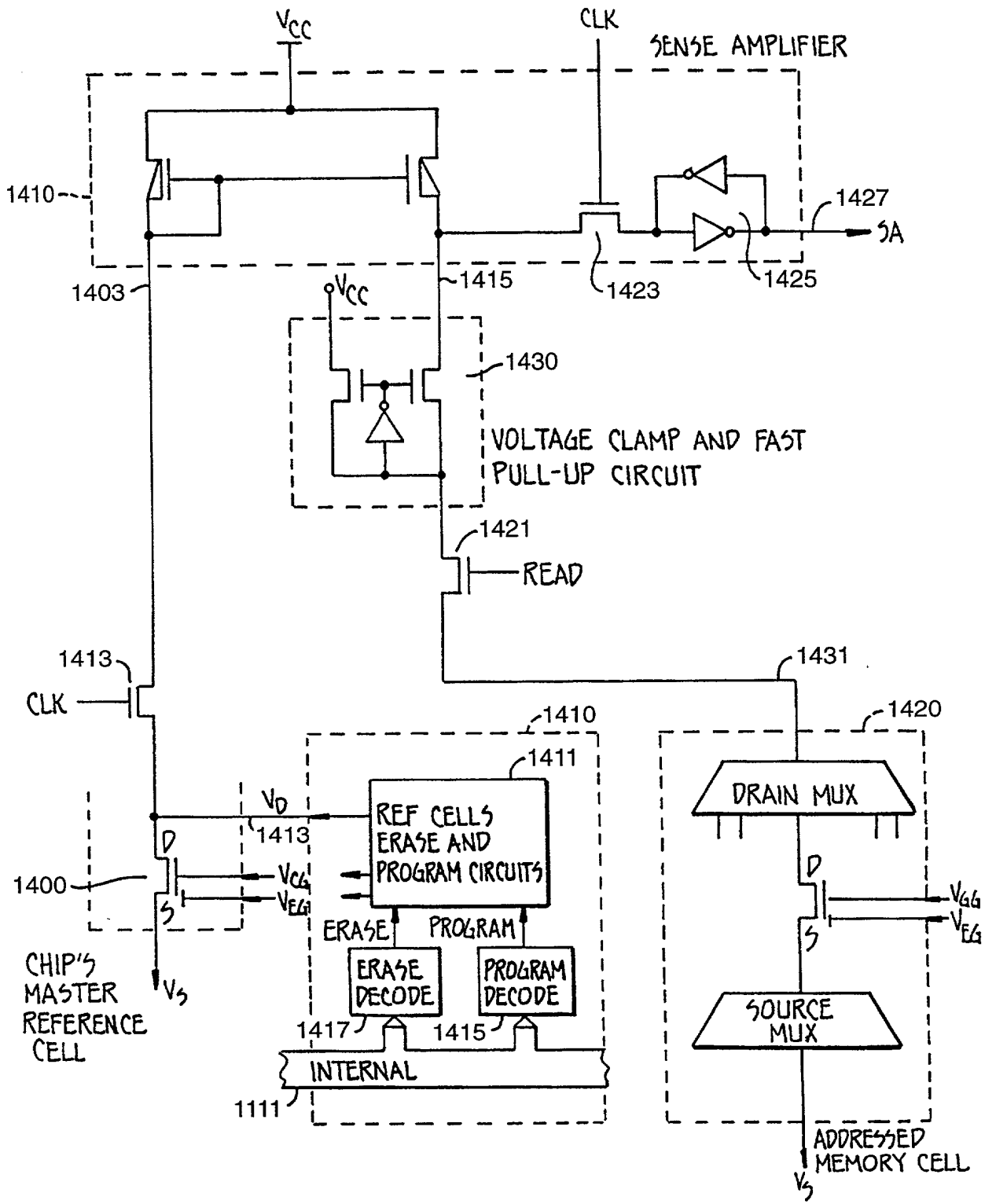


FIG. 17A

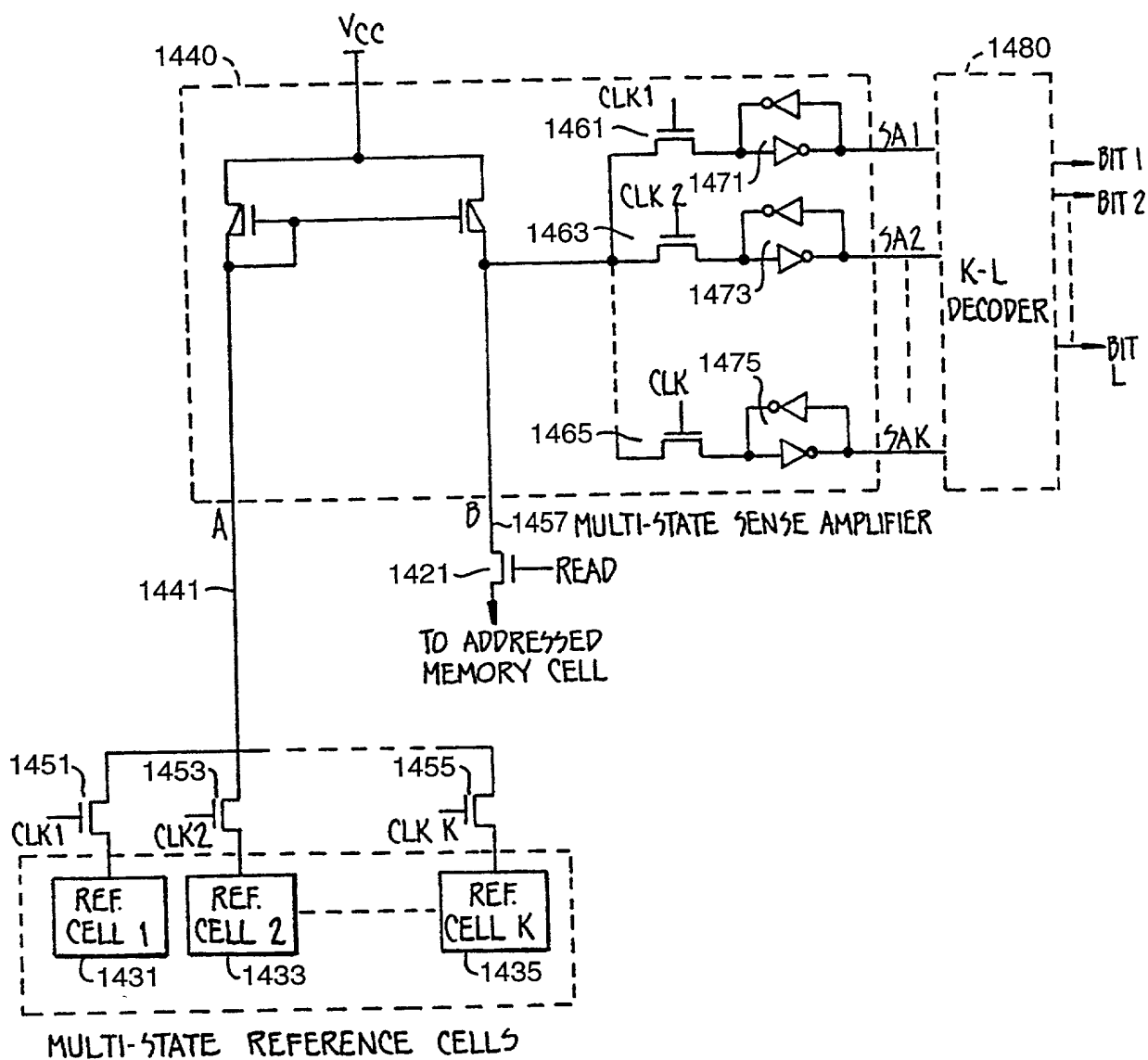
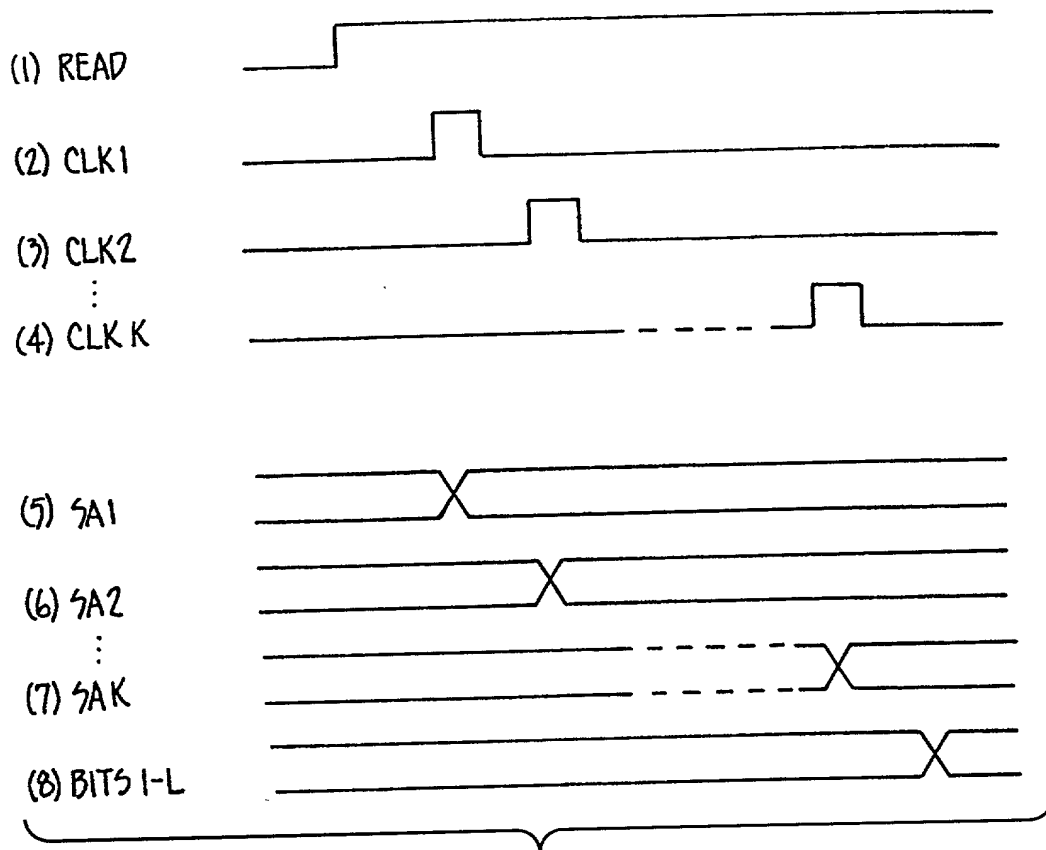
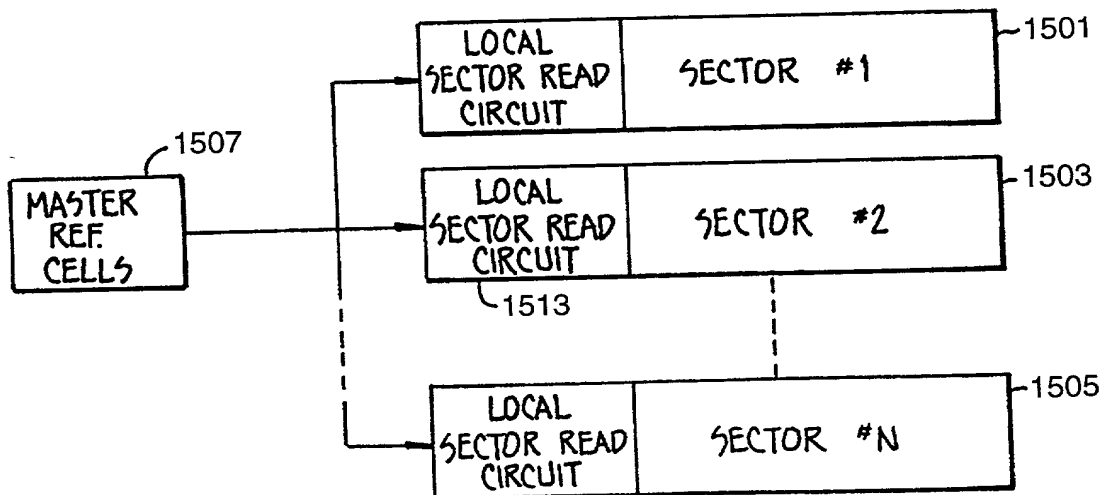


FIG. 17B



**FIG.\_17C**



**FIG.\_18**

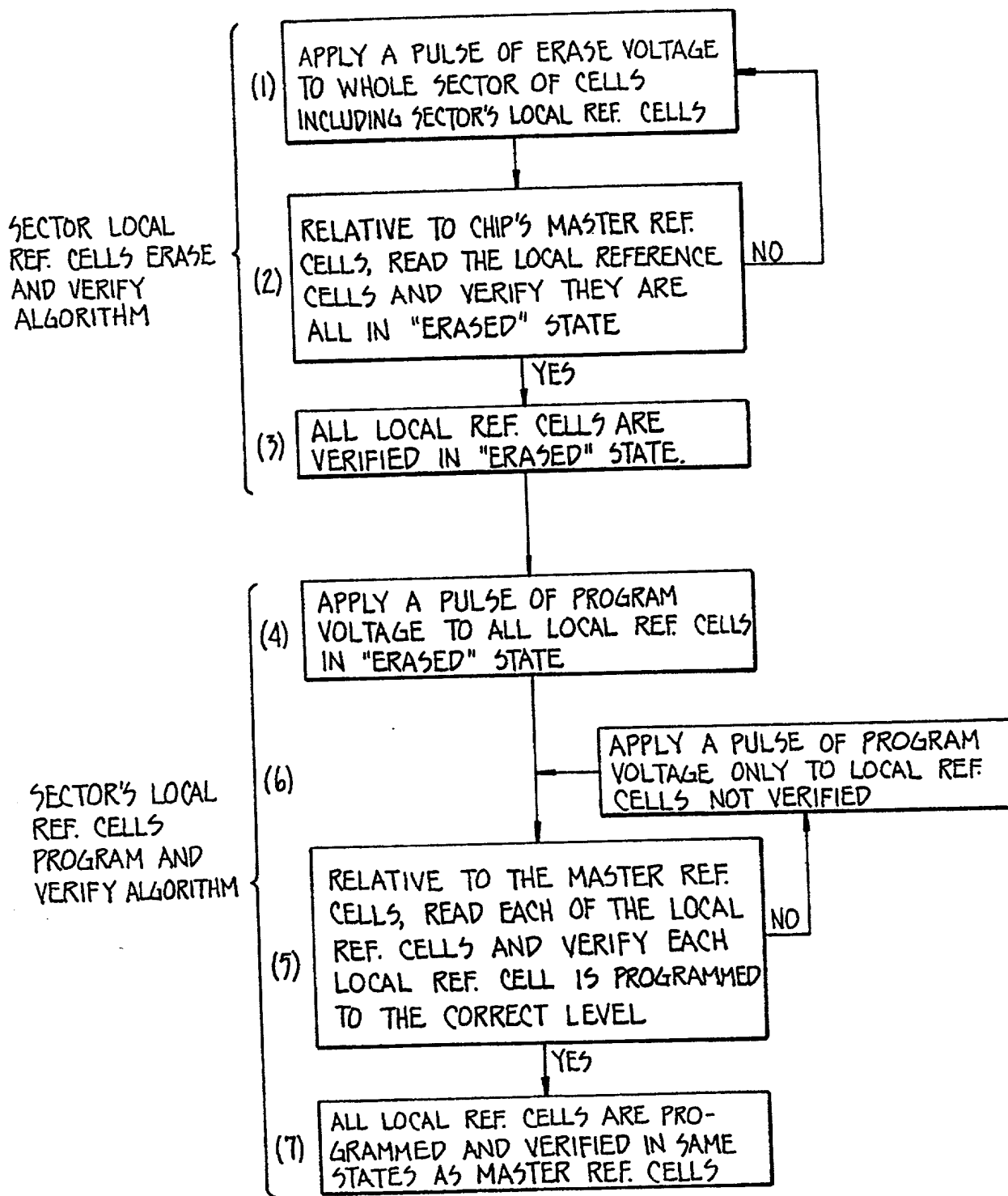
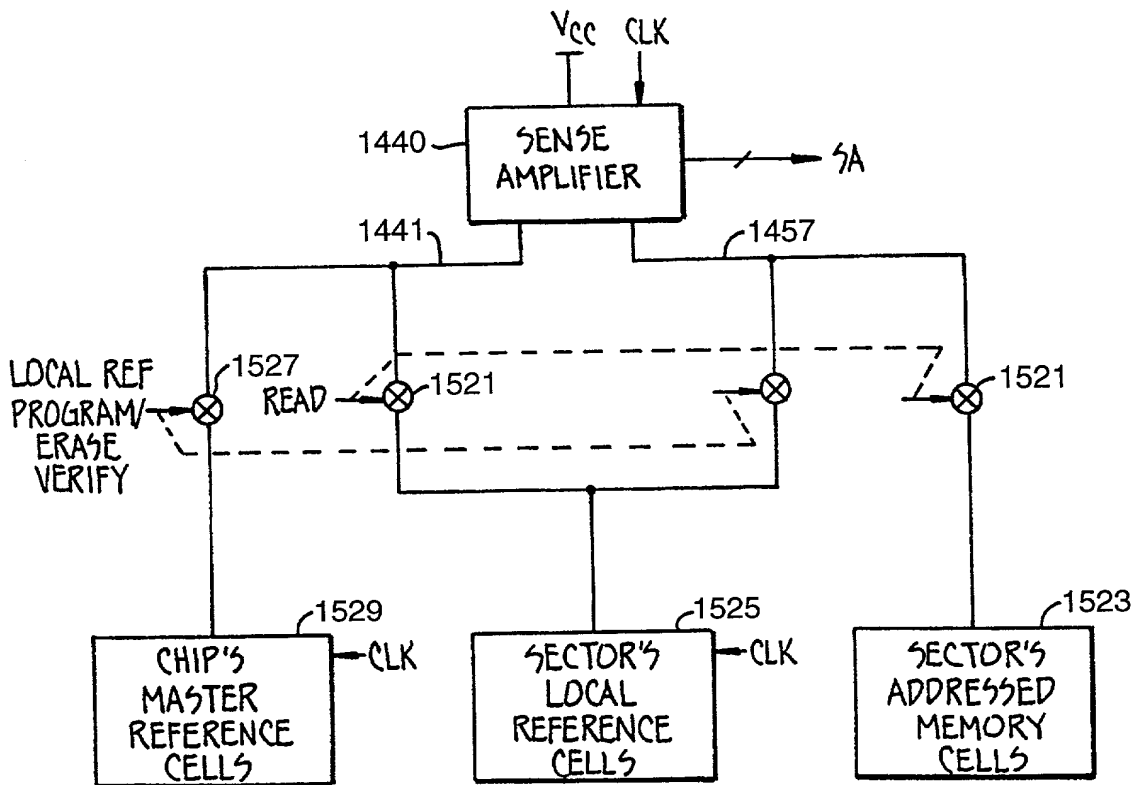
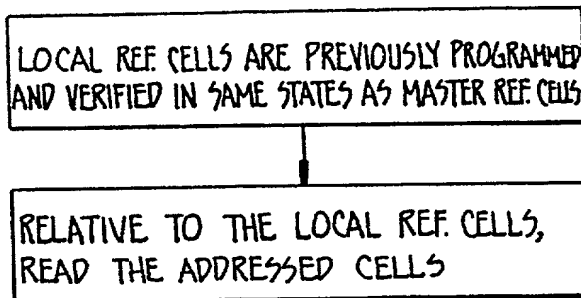


FIG. 19



**FIG. 20A**



**FIG. 20B**

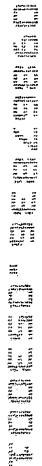
**FIG. 21A**

The diagram illustrates a sense amplifier circuit (FIG. 21A). At the top, a **SENSE AMPLIFIER** (1440) is shown with inputs for  $V_{cc}$  and **CLK** (1440). It has two outputs: **SA** and a signal line (1441). The signal line (1441) is connected to a crossbar (1533) and a read line (1535). The crossbar (1533) is connected to a **BIASED CHIP'S MASTER REFERENCE CELLS** (1531) and a **SECTOR'S LOCAL REFERENCE CELLS** (1525). The read line (1535) is connected to a **SECTOR'S ADDRESSED MEMORY CELLS** (1523). The **CLK** signal is also connected to the **BIASED CHIP'S MASTER REFERENCE CELLS** (1531), **SECTOR'S LOCAL REFERENCE CELLS** (1525), and **SECTOR'S ADDRESSED MEMORY CELLS** (1523).

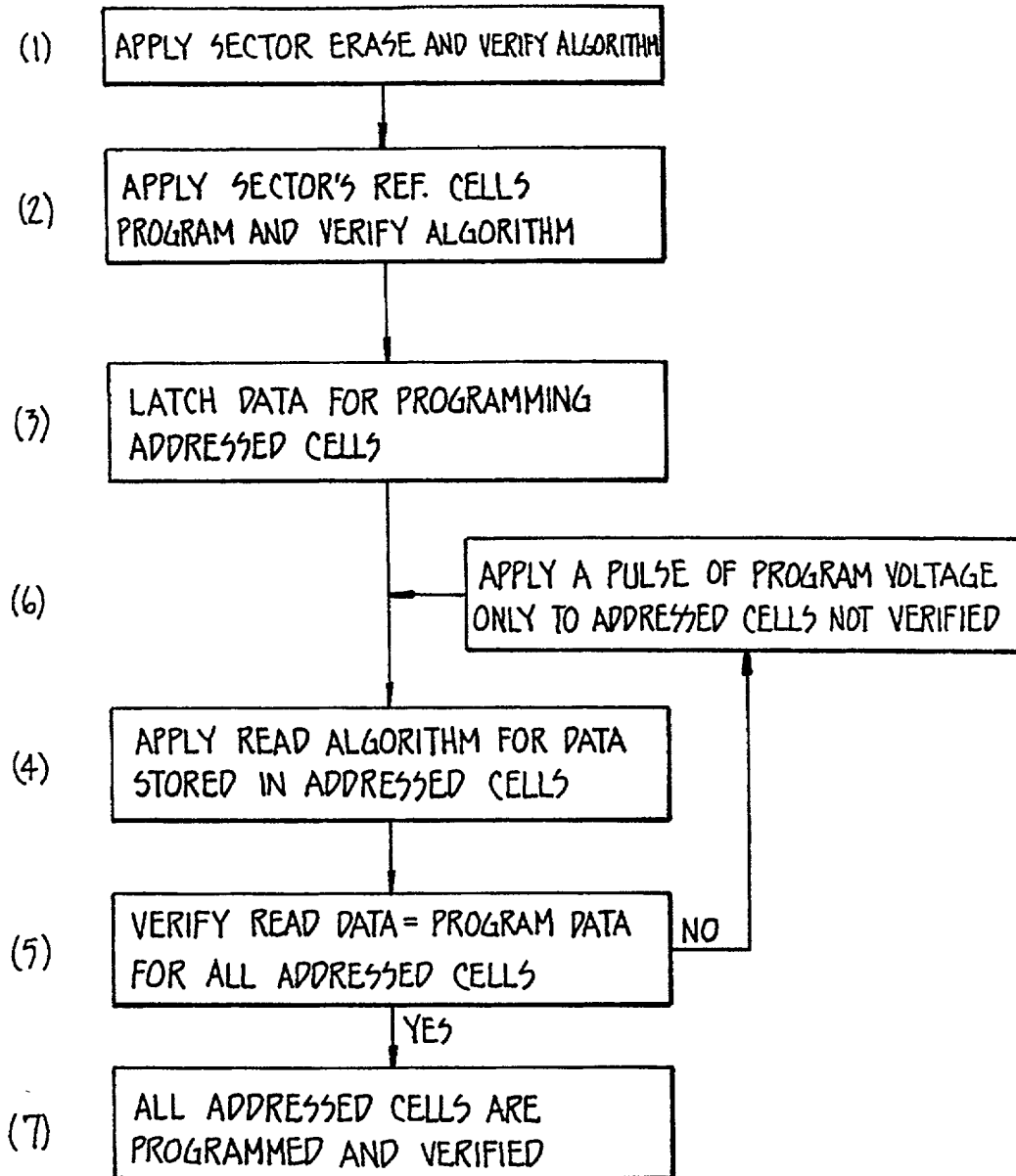






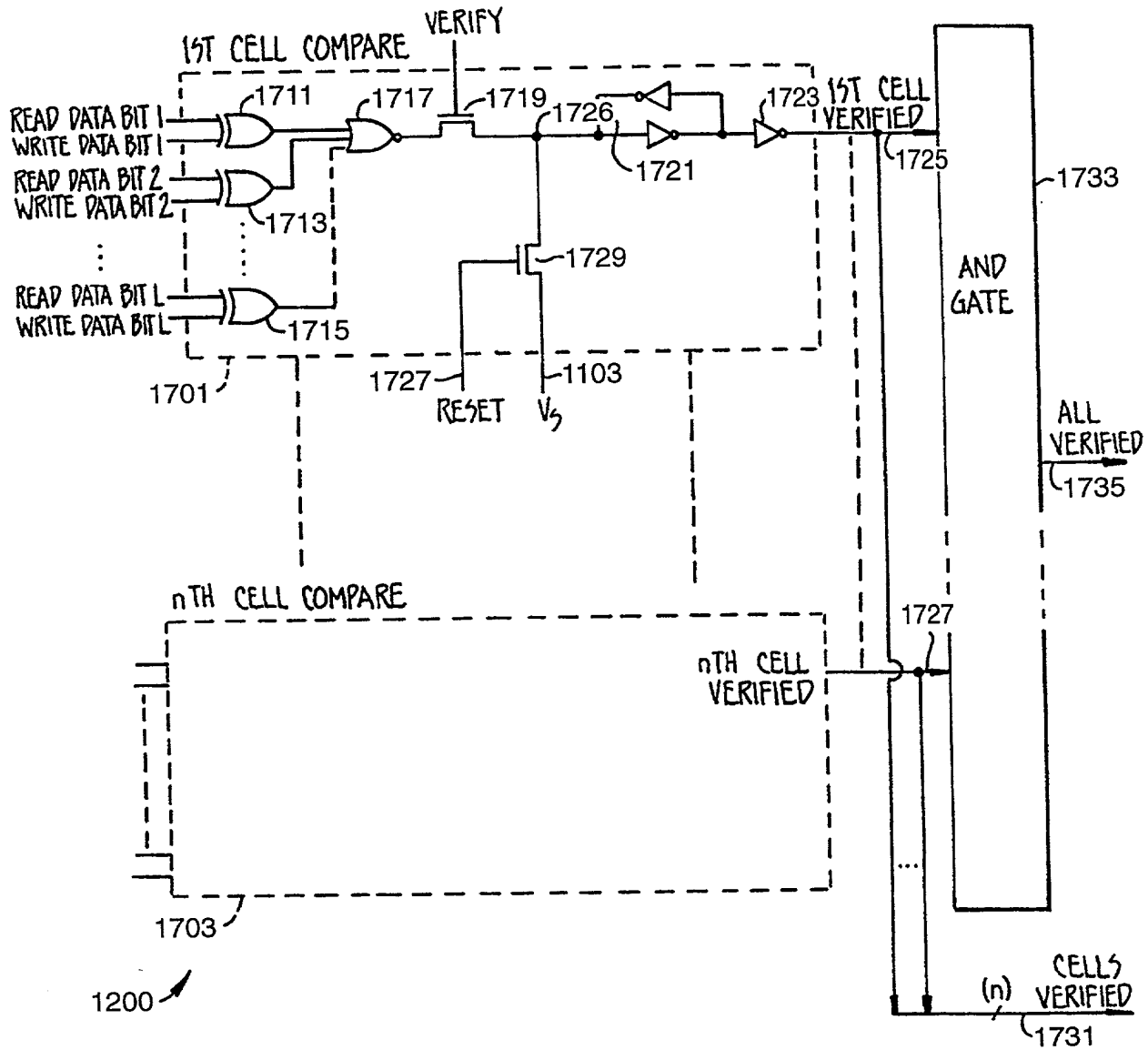


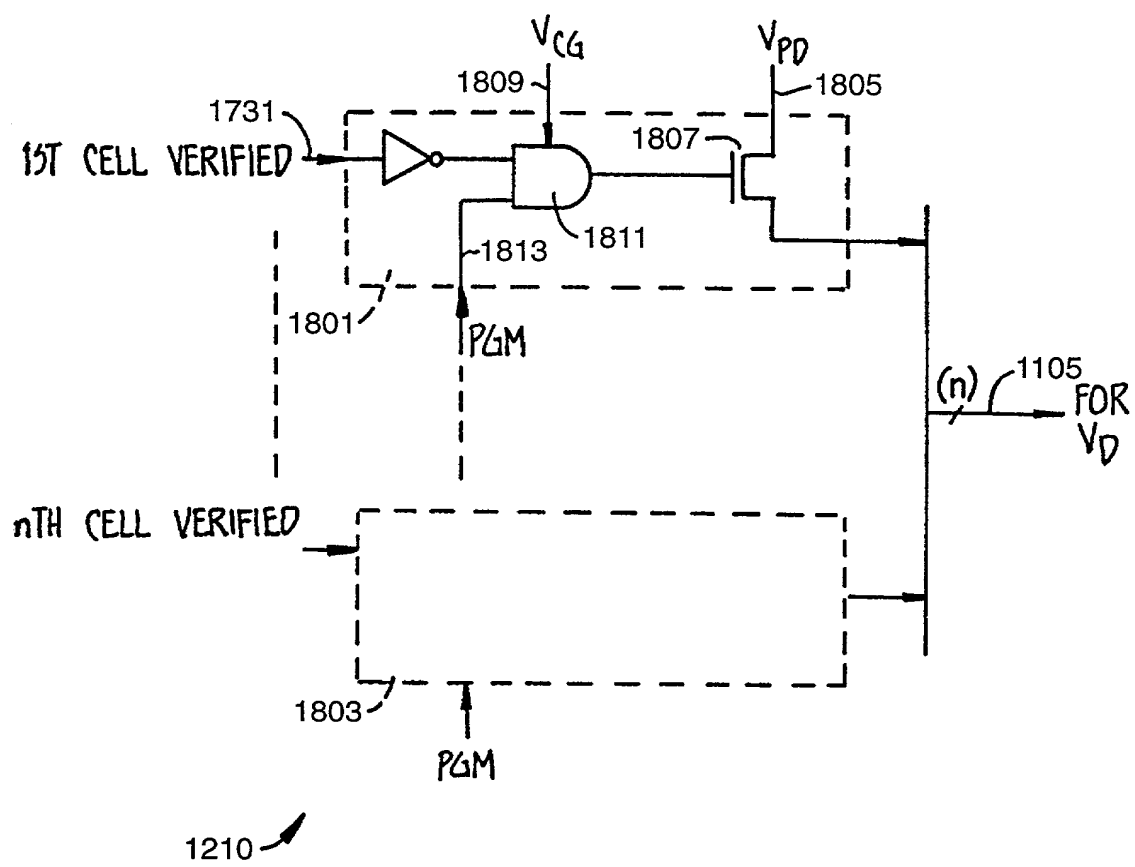
**FIG. 22**



PROGRAM ALGORITHM

**FIG.\_23**

**FIG. 24**



**FIG. 25**

	SELECTED CONTROL GATE $V_{CG}$	DRAIN $V_D$	SOURCE $V_S$	ERASE GATE $V_{EG}$
READ	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
PROGRAM	$V_{PG}$	$V_{PD}$	$V_{SS}$	$V_E$
PROGRAM VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$
ERASE VERIFY	$V_{PG}$	$V_{REF}$	$V_{SS}$	$V_E$

TABLE 1

**FIG.\_26**

(TYPICAL VALUES)	READ	PROGRAM	PROGRAM VERIFY	ERASE	ERASE VERIFY
$V_{PG}$	$V_{CC}$	12V	$V_{CC} + \delta V$	$V_{CC}$	$V_{CC} - \delta V$
$V_{CC}$	5V	5V	5V	5V	5V
$V_{PD}$	$V_{SS}$	8V	8V	$V_{SS}$	$V_{SS}$
$V_E$	$V_{SS}$	$V_{SS}$	$V_{SS}$	20V	$V_{SS}$
UNSELECTED CONTROL GATE	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$	$V_{SS}$
UNSELECTED BIT LINE	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$	$V_{REF}$

 $V_{SS} = 0V, \quad V_{REF} = 1.5V, \quad \delta V = 0.5V - 1V$ 

TABLE 2

**FIG.\_27**